

Diagram illustrating a 6-to-3 bit reduction network. The inputs are labeled VIN_5, VIN_4, VIN_3, VIN_2, VIN_1, and VIN_0. The outputs are labeled G3, H3, and H2. The network consists of several AND gates and OR gates. The output G3 is the OR of VIN_5, VIN_4, and VIN_3. The output H3 is the OR of VIN_5, VIN_4, and VIN_2. The output H2 is the OR of VIN_5, VIN_3, and VIN_1.

